GNHM4948LS

60 W, 48 V, 4.4–5.0 GHz GaN PA Module

Data Sheet V1.4

FEATURES

- Operating Frequency Range: 4.4 – 5.0 GHz
- Operating Drain Voltage: +48 V
- High Power and High Efficiency
- 50 Ω Input / Output
- Integrated Doherty Final Stage
- Saturated Power: 47.5 dBm
- PAE at 39 dBm avg.: 34%
- Gain at 39 dBm avg.: 28.5 dB
- ACPR w/o DPD at 39 dBm Avg.: -35 dBc
- ACPR w DPD at 39 dBm Avg.: -51 dBc
- 6 x 10 mm Plastic Surface Mount Package

Note: T = +25°C, 100 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF.

APPLIATIONS

- 5G Massive MIMO
- Macro-cell Base Station Driver
- Micro-cell Base Station
- General Purpose Applications

DESCRIPTION

Gaxtrem's GNHM4948LS is an integrated 2-stage Power Amplifier Module with 8-W average output power and 4.4 – 5.0-GHz operating frequency range. The module is 50 Ω input and output fully matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions. The module incorporates a Doherty final stage delivering high power added efficiency for the entire module at 8-W average output power.

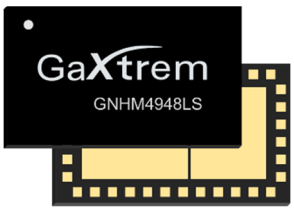


Figure 2. 36 Pad 6 x 10 mm Plastic LGA Package

The GNHM4948LS is part of a high-efficiency, pin-to-pin compatible PA family supporting major 3GPP bands. Table 1 lists the pin-to-pin compatible parts in the PA family.

A block diagram of the GNHM4948LS is shown in Figure 1. The device package and pinout for the device are shown in Figure 2 and Figure 3, respectively. Signal pin assignments and functional pin descriptions are described in Table 2.

Table 1. Pin-to-Pin Compatible PA Family

Part Number	Frequency (GHz)	3GPP Band
GNHM3551LB	3.3 to 3.8	Band n78
GNHM3551LE	3.3 to 3.6	Band n78
GNHM3549LB	3.3 to 3.8	Band n78
GNHM3549LN	3.3 to 3.6	Band n78
GNHM4949LB	4.4 to 5.0	Band n79
GNHM4949LN	4.8 to 5.0	Band n79
GNHM4948LS	**4.4 to 5.0**	**Band n79**
GNNM4945LA	4.4 to 5.0	Band n79

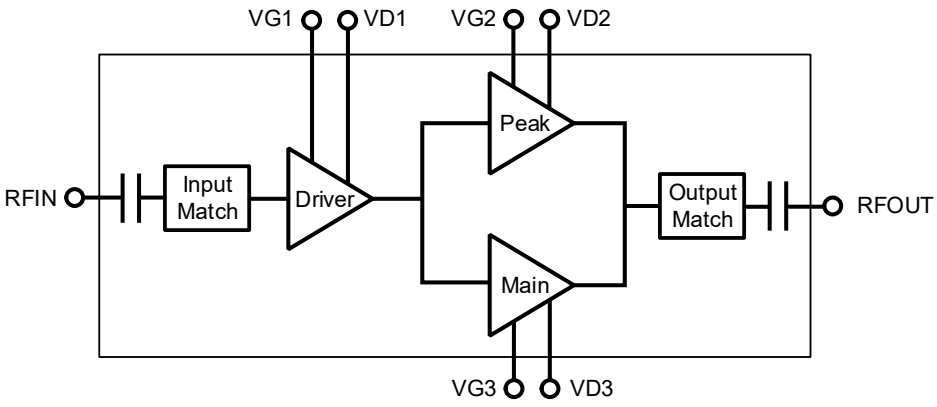


Figure 1. GNHM4948LS Block Diagram

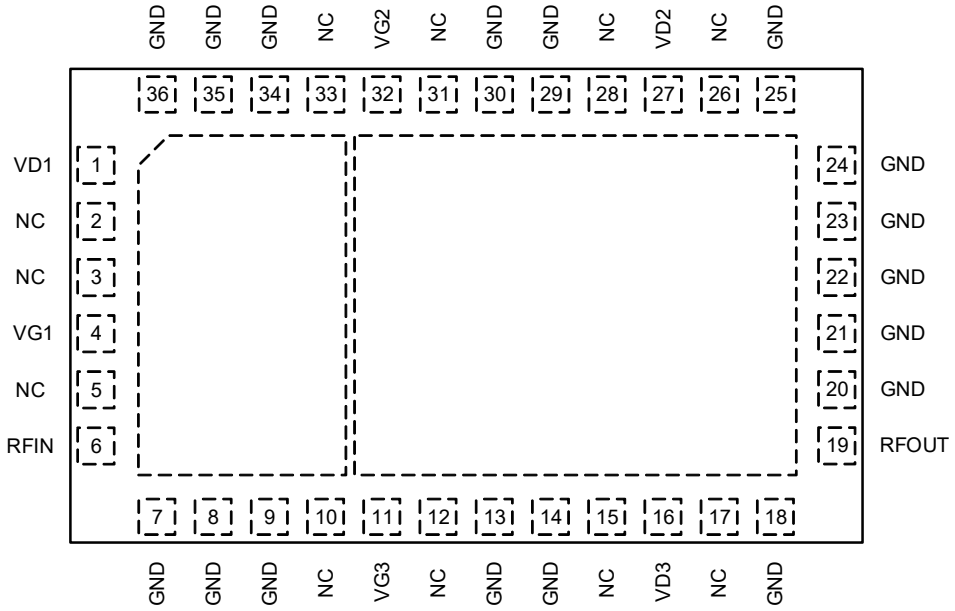


Figure 3. GNHM4948LS Pinout (Top View)

Table 2. GNHM4948LS Signal Descriptions

Pin	Name	Description
1	VD1	Driver Amplifier, Drain Bias
4	VG1	Driver Amplifier, Gate Bias
6	RFIN	RF Input
11	VG3	Main Amplifier, Gate Bias
16	VD3	Main Amplifier, Drain Bias, Connected to VD2 internally
19	RFOUT	RF Output
27	VD2	Peak Amplifier, Drain Bias, Connected to VD3 internally
32	VG2	Peaking Amplifier, Gate Bias
2-3, 5, 10, 12, 15, 17, 26, 28, 31, 33	NC	No Connection
7-9, 13-14, 18, 20-25, 29-30, 34-36	GND	Internal Grounding. Recommend connecting to Epad ground.
EPAD	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under EPAD will result in excessive junction temperatures causing permanent damage.

ELECTRIAL SPECIFICATIONS

The following tables list the electrical characteristics of the GNHM4948LS PA Module. Table 3 lists the absolute maximum ratings and Table 4 lists the recommended operating conditions. Electrical specifications are provided in Table 5. Typical performance characteristics are shown in Figure 4, Figure 5, Figure 6, Table 7 and Table 8. GNHM4948LS is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields.

Table 3. Absolute Maximum Rating

Parameter	Value	Unit
Breakdown Voltage (BVDG)	200	V
Gate Voltage (VG1, VG2, VG3)	-8 to +0.6	V
Drain Voltage (VD1, VD2, VD3)	+55	V
VSWR Mismatch (20 MHz LTE signal, 10-dB PAR, 39-dBm average power for VSWR 1:1, T = +25°C)	10:1	
Storage Temperature Range	-65 to +150	℃
Case Operating Temperature	+150	℃
Operating Junction Temperature	+225	℃

Table 4. Recommended Operating Conditions

Parameter	Value			Unit
	Min.	Typ.	Max.	
Gate Voltage (VG1)	-3.3	-3.1	-2.8	V
Gate Voltage (VG2)	-4.9	-4.4	-4.0	V
Gate Voltage (VG3)	-3.3	-3.15	-2.8	V
Drain Voltage (VD1, VD3)		48		V
Quiescent Current (IDQ1)		35		mA
Quiescent Current (IDQ3)		78		mA

Table 5. Electrical Specifications

Parameter	Value			Unit	Condition
	Min.	Typ.	Max.		
Frequency Range	4.4		5.0	GHz	
Driver Quiescent Current (IDQ1)		35		mA	
Main Quiescent Current (IDQ3)		78		mA	
Gain at 39 dBm avg.	25.5	28.5		dB	
PAE at 39 dBm avg.	32	34		%	
ACPR w/o DPD at 39 dBm avg.		-35		dBc	
ACPR w DPD at 39 dBm avg.		-51		dBc	
Saturated output power	47.2	47.5		dBm	Pulse CW (20us/200us)

Test conditions unless otherwise noted: VD1,3 = +48 V, IDQ1 = 35 mA, IDQ3 = 78 mA, VG2 = −4.4 V, T = +25°C, using a single-carrier, 100 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF on the reference design fixture.

Table 6. Thermal Information

Parameter	Value	Unit	Condition
Thermal Resistance at Average Power, Junction to Case	4.9	℃/W	Tcase = +85℃, Tch = 168℃ CW : Pdiss = 17 W, Pout = 8W

Notes:

1. The thermal resistance is acquired by Gaxtrem's FEA model.
2. The reference Tcase temperature 85℃ is applied on the backside of package.
3. The power dissipation in the table is the overall dissipation of Main PA, Peaking PA and Driver PA.

TYPICAL PERFORMANCE PLOTS

(VD1,3 = +48 V, IDQ1 = 35 mA, IDQ3 = 78 mA, VG2 = −4.4 V, T=25℃)

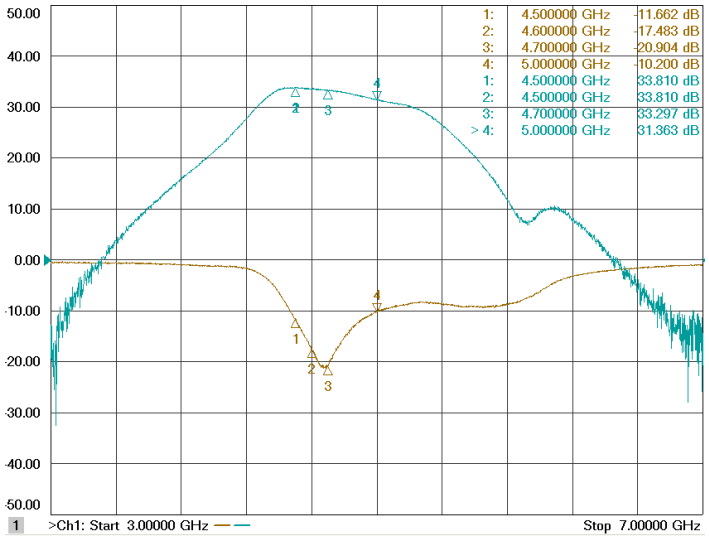


Figure 4. Measured S-parameters from 3 to 7 GHz

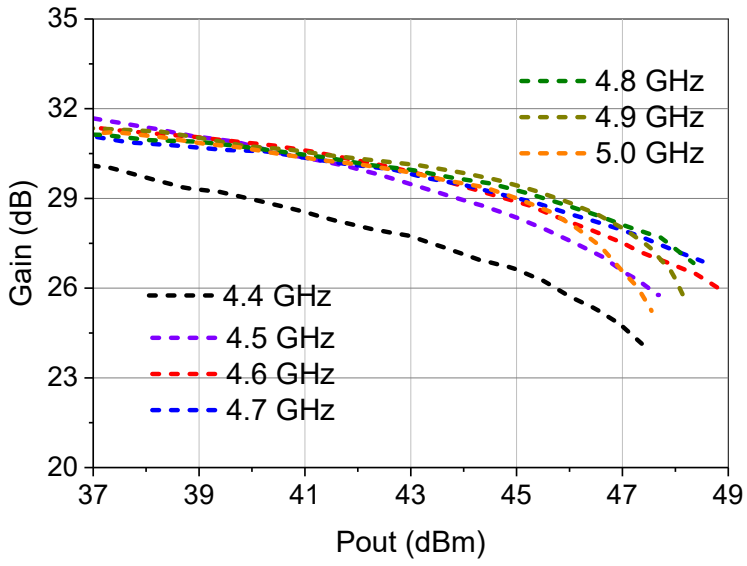


Figure 5. Measured Gain Versus Output Power (Pulse CW, 20us Pulse Width, 10% Duty Cycle)

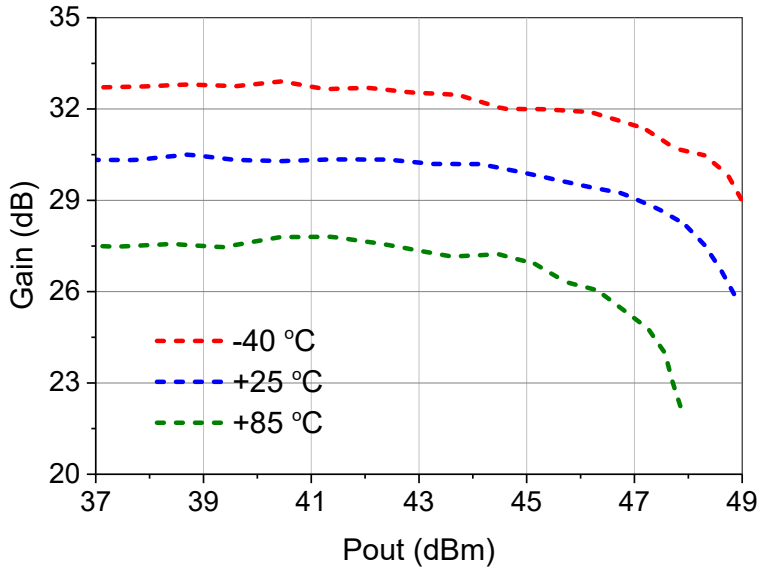


Figure 6. Measured Gain Versus Output Power Across Temperature at 4.9 GHz (Pulse CW, 20us Pulse Width, 10% Duty Cycle)

Table 7. Measured Performance under a pulse CW (summary of Figure 5)

Freq (GHz)	Psat (dBm)	Gain at 39 dBm (dB)	Gain at Psat dBm (dB)
4.4	47.4	29.3	24.2
4.5	47.7	31.1	25.8
4.6	48.8	31.1	26.0
4.7	48.5	30.7	26.9
4.8	48.3	30.9	26.8
4.9	48.1	31.0	25.7
5.0	47.6	30.8	25.3

Table 8. Measured Performance under a 100 MHz LTE signal with 8.5-dB PAR

Freq (GHz)	Pout (dBm)	ACPR w/o DPD (dBc)	ACPR w DPD (dBc)	PAE (%)	Gain (dB)
4.45	39	-31.4/-32.9	-51.7/-49.3	32.4	25.5
4.55	39	-35.6/-35.4	-51.3/-50.8	32.7	27.8
4.65	39	-33.4/-36.2	-51.6/-51.8	33.2	28.3
4.75	39	-32.2/-34	-51.7/-52	33.5	28.5
4.85	39	-33.7/-34.7	-52/-52.6	34	28.5
4.95	39	-34.5/-35.2	-51.6/-52.6	33.6	28

REFERENCE DESIGN

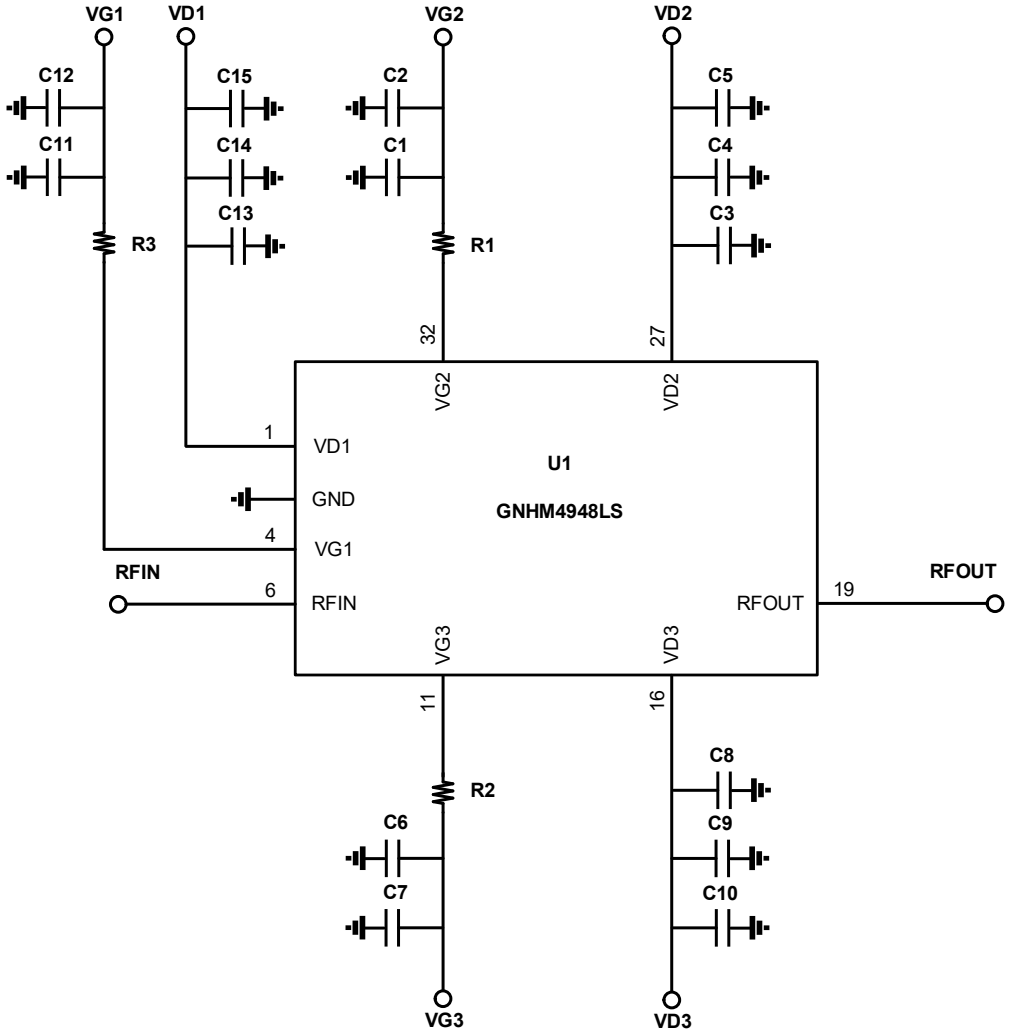


Figure 7. GNHM4948LS Application Schematic

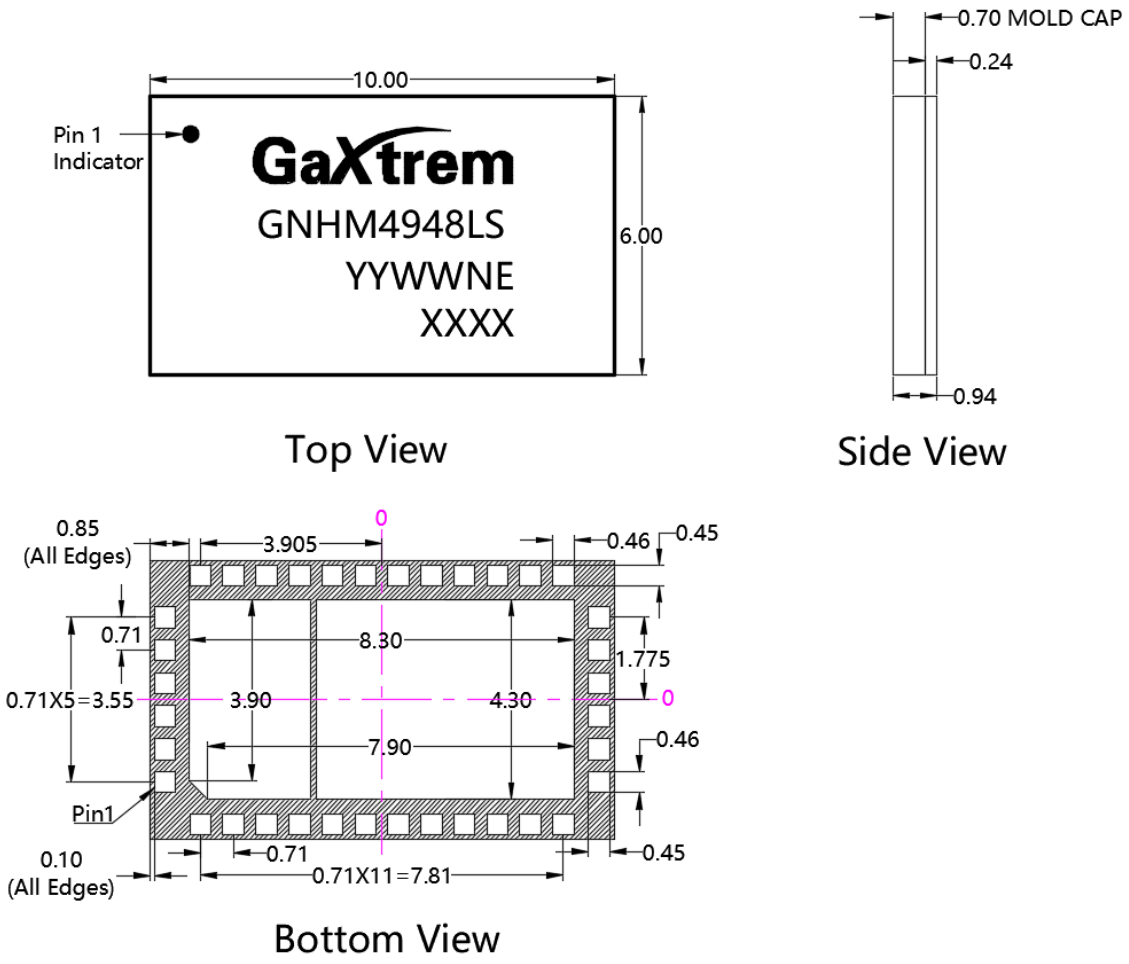
Table 9. GNHM4948LS Evaluation Board Bill of Materials (BOM)

Component	Description	Manufacturer	Part Number
C1, C3, C6, C8, C11, C13	Capacitor, 10 nF, 50 V, 0603	Murata	GRM188R71H103KA01
C4, C9, C14	Capacitor, 22 nF, 100 V, 0805	Yageo	CC0805KRX7R0BB223
C2, C7, C12	Capacitor, 10 uF, 16 V, 0603	Murata	GRM188R61C106KAALD
C5, C10, C15	Capacitor, 10 uF, 63 V, 1210	Murata	GRM32ER71J106KA12L
R1, R2, R3	Resistor, 10R, 0402	Yageo	RC0402FR-071RL
U1	60W, 4.4-5.0 GHz GaN PA Module	Gaxtrem	GNHM4948LS

Notes:

1. The device is soldered on a 20mil Rogers 4350 PCB.
2. For TDD operation, C2, C7, and C12 should be removed to increase the switching speed of the gate bias.
3. VD2 can be left unconnected, as it is connected to VD3 internally.
4. Gerber file of EVB layout can be provided based on request.

PACKAGE MARKING AND DIMENSIONS



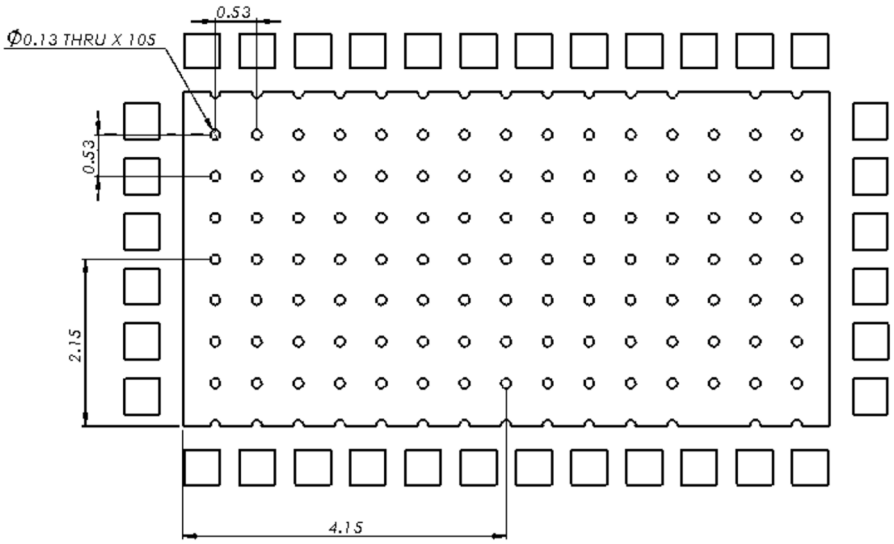
Notes:

1. All dimensions are in millimeters.

2. Exposed metallization is NiPdAu plated.

Figure 8. GNHM4948LS Package Dimension

MOUNTING FOOTPRINT PATTERN



Notes:

1. All dimensions are in millimeters. Angles are in degrees.

2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. All vias are plated thru hole (PTH) to ground.

Figure 9. GNHM4948LS PCB Layout Footprint

RECOMMENDED SOLDER TEMPERATURE PROFILE

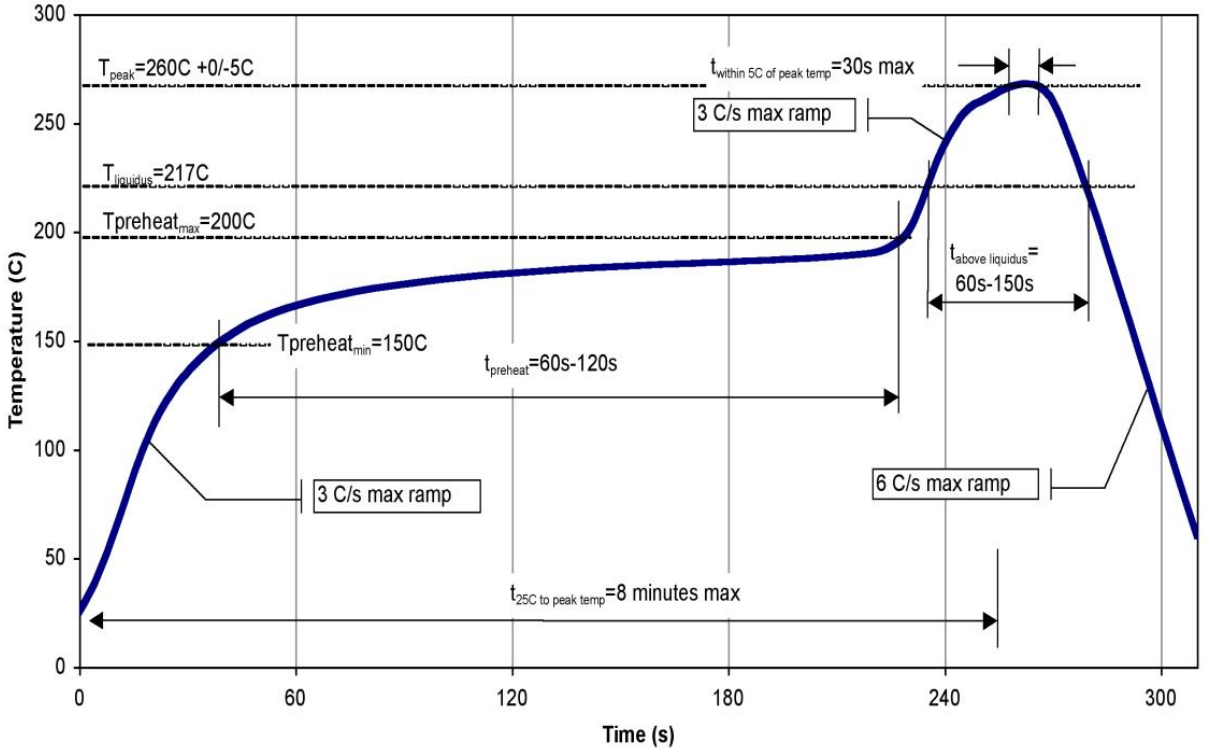


Figure 10. Recommended Solder Temperature Profile

HANDLING PRECAUTIONS

Table 10. ESD Sensitivity

Parameter	Rating	Standard
Human Body Model (HBM)	± 250V (Class 1A)	JEDEC Standard JS-001-2017
Charged Device Model (CDM)	± 2000V (Class C3)	JEDEC Standard JS-002-2018

SOLDERABILITY

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiAu

RoHS COMPLIANCE

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

REVISION HISTORY

Table 11. Document Revision History

Date	Revision	Datasheet Status
2022/3/25	Rev 1.0	Preliminary Datasheet
2022/4/29	Rev 1.1	Update measurement results
2022/11/23	Rev 1.2	Update package marking; add thermal resistance
2023/2/14	Rev 1.3	Add ESD characteristics, and gain vs power across temperature.
2023/6/22	Rev 1.4	Update measurement results; add VSWR mismatch