FEATURES

- Operating Frequency Range: 3.3 – 3.6 GHz
- Operating Drain Voltage: +28 V
- High Power and High Efficiency
- 50 Ω Input / Output
- Integrated Doherty Final Stage
- Saturated Power: 41.5 dBm
- PAE at 33 dBm avg: 40%
- Gain at 33 dBm avg: 28.5 dB
- ACPR w/o DPD at 33 dBm Avg: -35 dBc
- ACPR w DPD at 33 dBm Avg: -48 dBc
- 8 x 8 mm Plastic Surface Mount Package

Note: T = +25°C, 100 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF.

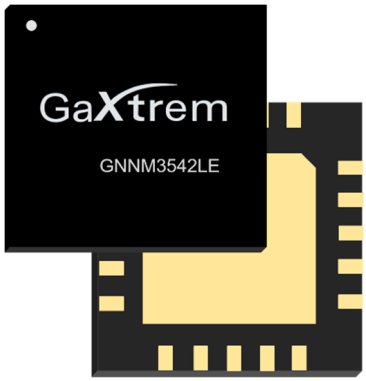

Figure 1. 20 Pad 8 x 8 mm Plastic LGA Package

APPLICATIONS

- 5G Massive MIMO
- Macro-cell Base Station Driver
- Small-cell Base Station
- General Purpose Applications

DESCRIPTION

Gaxtrem's GNNM3542LE is an integrated 2-stage Power Amplifier Module with 2-W average output power and 3.3 – 3.6GHz operating frequency range. The module is 50 Ω input and output and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions. The module incorporates a Doherty final stage delivering high power added efficiency for the entire module at 2-W average output power.

A block diagram of the GNNM3542LE is shown in Figure 2. The device package and pinout for the device are shown in Figure 3. Signal pin assignments and functional pin descriptions are described in Table 1.

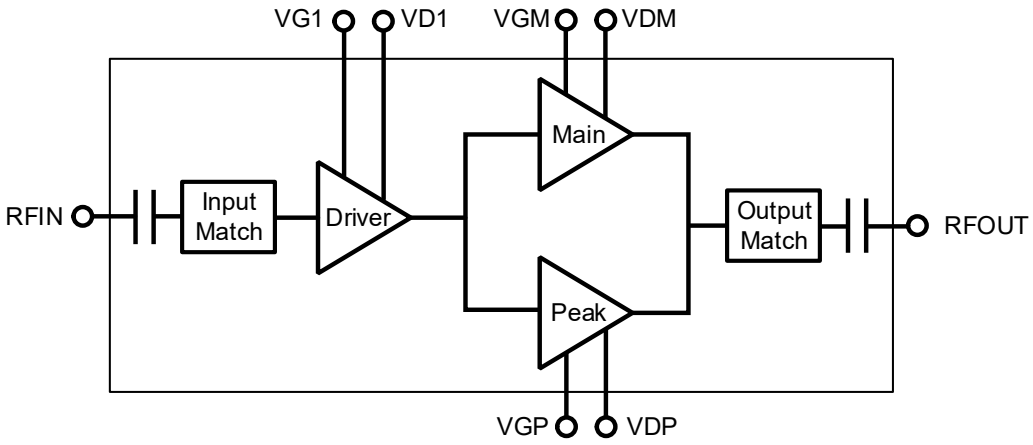

Figure 2. GNNM3542LE Block Diagram

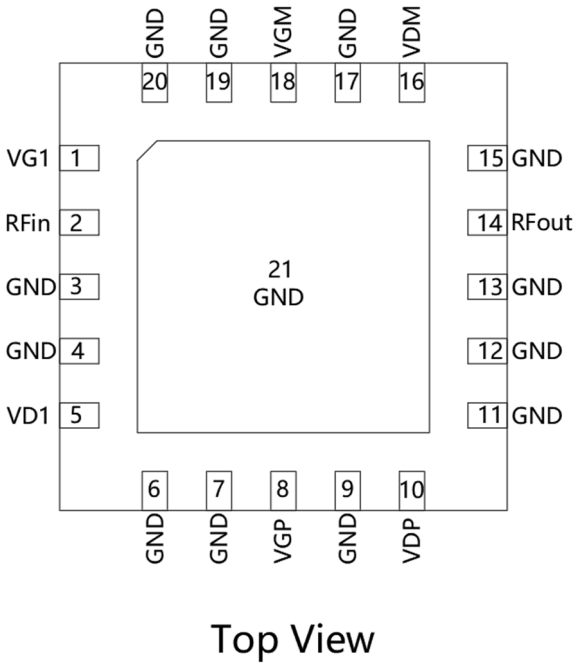

Figure 3. GNNM3542LE Pinout (Top View)

Table 1. GNNM3542LE Signal Descriptions

Pin	Name	Description
1	VG1	Driver Amplifier, Gate Bias
2	RFin	RF Input
5	VD1	Driver Amplifier, Drain Bias
8	VGP	Peak Amplifier, Gate Bias
10	VDP	Peak Amplifier, Drain Bias
14	RFOUT	RF Output
16	VDM	Main Amplifier, Drain Bias
18	VGM	Main Amplifier, Gate Bias
3-4, 6-7, 9, 11-13, 15, 17、19-20	GND	Internal Grounding. Recommend connecting to Epad ground.
21	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under EPAD will result in excessive junction temperatures causing permanent damage.

ELECTRICAL SPECIFICATIONS

The following tables list the electrical characteristics of the GNNM3542LE PA Module. Table 2 lists the absolute maximum ratings and Table 3 lists the recommended operating conditions. Electrical specifications are provided in Table 4. Typical performance characteristics are shown in Fig. 4, Fig. 5, Table 6. GNNM3542LE is a static-sensitive electronic device and should not be stored or operated near strong electrostatic fields.

Table 2. Absolute Maximum Rating

Parameter	Value	Unit
Breakdown Voltage (BVDG)	120	V
Gate Voltage (VG1, VGM, VGP)	-8 to +0.6	V
Drain Voltage (VD1, VDM, VDP)	+32	V
VSWR Mismatch (20 MHz LTE signal, 10-dB PAR, 33-dBm average power for VSWR 1:1, T = +25°C)	10:1	
Storage Temperature Range	-65 to +150	℃
Case Operating Temperature	+150	℃
Operating Junction Temperature	+225	℃

Table 3. Recommended Operating Conditions

Parameter	Value			Unit
	Min.	Typ.	Max.	
Gate Voltage (VG1)	-2.5	-2.17	-2	V
Gate Voltage (VGP)	-3.6	-3.3	-3.0	V
Gate Voltage (VGM)	-2.5	-2.21	-2	V
Drain Voltage (VD1, VDP,VDM)		28	32	V
Quiescent Current (IDQ1)		13.5		mA
Quiescent Current (IDQM)		31		mA

Table 4. Electrical Specifications

Parameter	Value			Unit	Condition
	Min.	Typ.	Max.		
Frequency Range	3.3		3.6	GHz	
Driver Quiescent Current (IDQ1)		13.5		mA	
Main Quiescent Current (IDQM)		31		mA	
Gain at 33 dBm avg.	28	28.5		dB	
PAE at 33 dBm avg.	38	40		%	
ACPR w/o DPD at 33 dBm avg.		-35		dBc	
ACPR w DPD at 33 dBm avg.		-48		dBc	
Saturated output power		41.5		dBm	Pulse CW (20us/200us)

Test conditions unless otherwise noted: VD = +28 V, IDQ1 = 13.5 mA, IDQM = 31 mA, VGP = −3.3 V, T = +25°C, using a single-carrier, 100 MHz LTE signal with 8.5 dB PAR at 0.01% CCDF on the reference design fixture. DPD results are acquired by Gaxtrem's DPD test bench.

Table 5. Thermal Information

Parameter	Value	Unit	Condition
Thermal Resistance at Average Power, Junction to Case	13	℃/W	Tcase = +85℃, Tch = 124℃ CW: Pdiss=3W, Pout=2W

Notes:

1. The thermal resistance is acquired by Gaxtrem's FEA model.
2. The reference Tcase temperature 85℃ is applied on the backside of package.
3. The power dissipation in the table is the overall dissipation of Main PA, Peaking PA and Driver PA.

TYPICAL PERFORMANCE PLOTS

(VD1,P,M= +28 V, IDQ1 = 13.5mA, IDQM = 31 mA, VGP = −3.3 V, T=25℃)

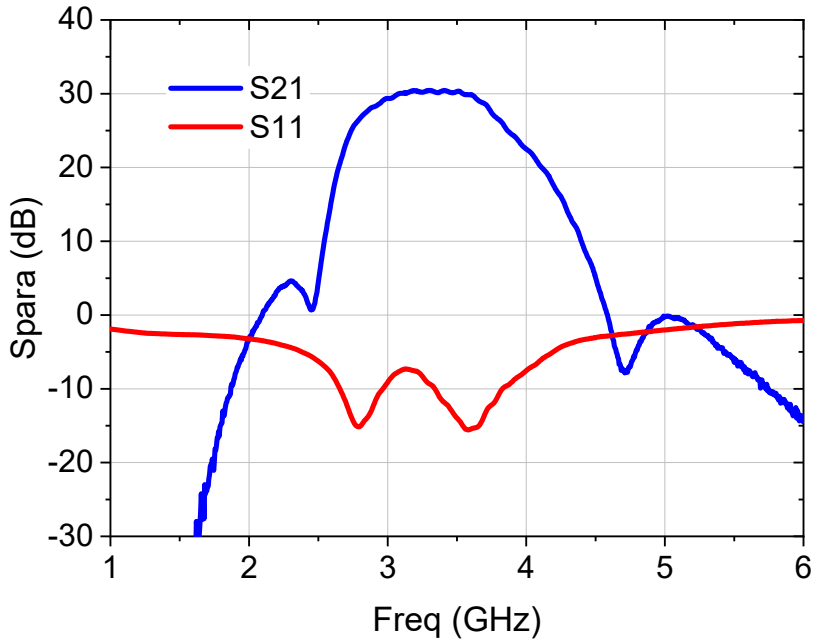

Figure 4. Measured S-parameters from 1 to 6 GHz

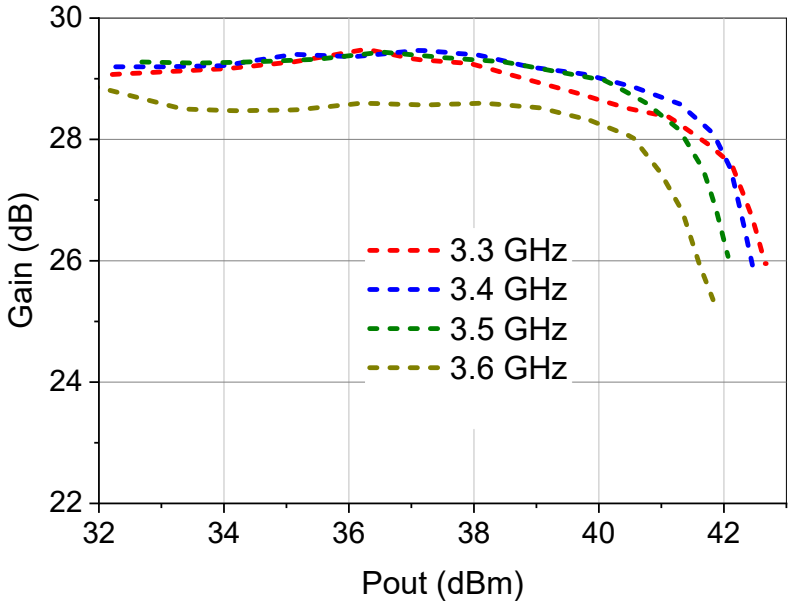

Figure 5. Measured Gain Versus Output Power (Pulse CW, 20us Pulse Width, 10% Duty Cycle)

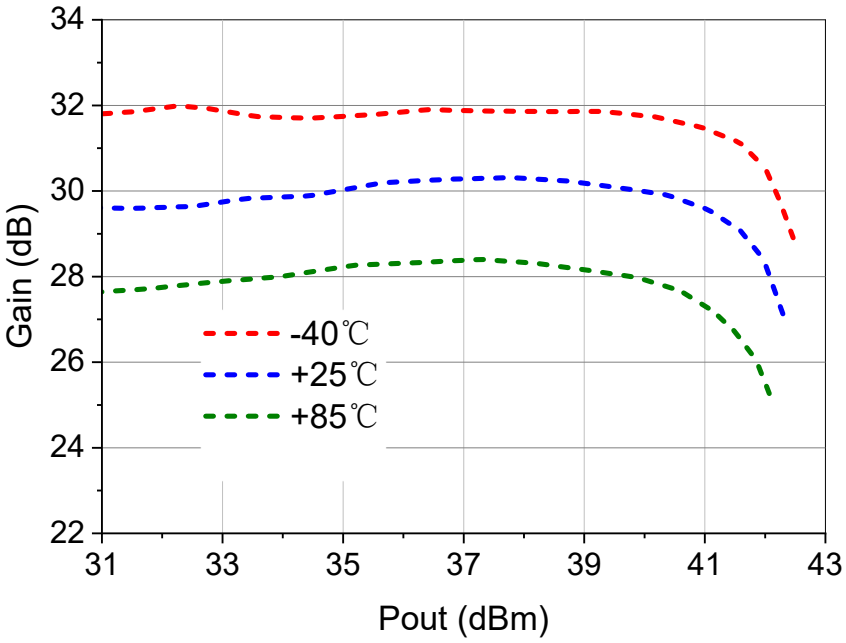

Figure 6. Measured Gain Versus Output Power Across Temperature at 3.45 GHz (Pulse CW, 20us Pulse Width, 10% Duty Cycle)

Table 6. Measured Performance under a pulse CW (summary of Figure 5)

Freq (GHz)	Psat (dBm)	Gain at 33 dBm (dB)	Gain at Psat dBm (dB)
3.3	42.6	29.1	26
3.4	42.4	29.2	25.9
3.5	42	29.2	26
3.6	41.8	28.5	25.3

Table 7. Measured Performance under a 100 MHz LTE signal with 8.5-dB PAR

Freq (GHz)	Pout (dBm)	ACPR w/o DPD (dBc)	ACPR w DPD (dBc)	PAE (%)	Gain (dB)
3.35	33	-41.1/-36.2	-52/-51.3	38.5	28.6
3.45	33	-41/-35.6	-51.4/-50	39.1	28.7
3.55	33	-38.7/-35.9	-49.8/-48	40.7	28.6

REFERENCE DESIGN

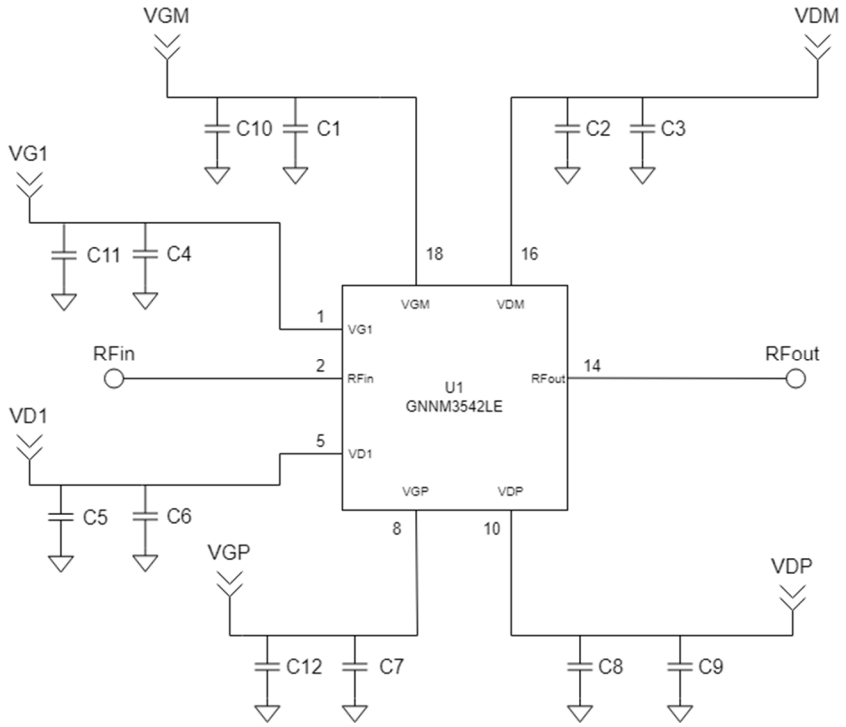

Figure 7. GNNM3542LE Application Schematic

Table 8. GNNM3542LE Evaluation Board Bill of Materials (BOM)

Component	Description	Manufacturer	Part Number
C1, C2, C4, C6, C7, C8	Capacitor, 10 nF, 50 V, 0603	Murata	GRM188R71H103KA01
C3, C5, C9	Capacitor, 10 uF, 63 V, 1210	Murata	GRM32ER71J106KA12L
C10, C11, C12	Capacitor, 10 uF, 16 V, 0603	Murata	GRM188R61C106KAALD
U1	15W, 3.3-3.6 GHz GaN PA Module	Gaxtrem	GNNM3542LE

Note:

1. The device is soldered on a 20mil Rogers 4350 PCB.
2. For TDD operation, C10, C11, and C12 should be removed to increase the switching speed of the gate bias.
3. Gerber file of EVB layout can be provided based on request.

PACKAGE DIMENSIONS

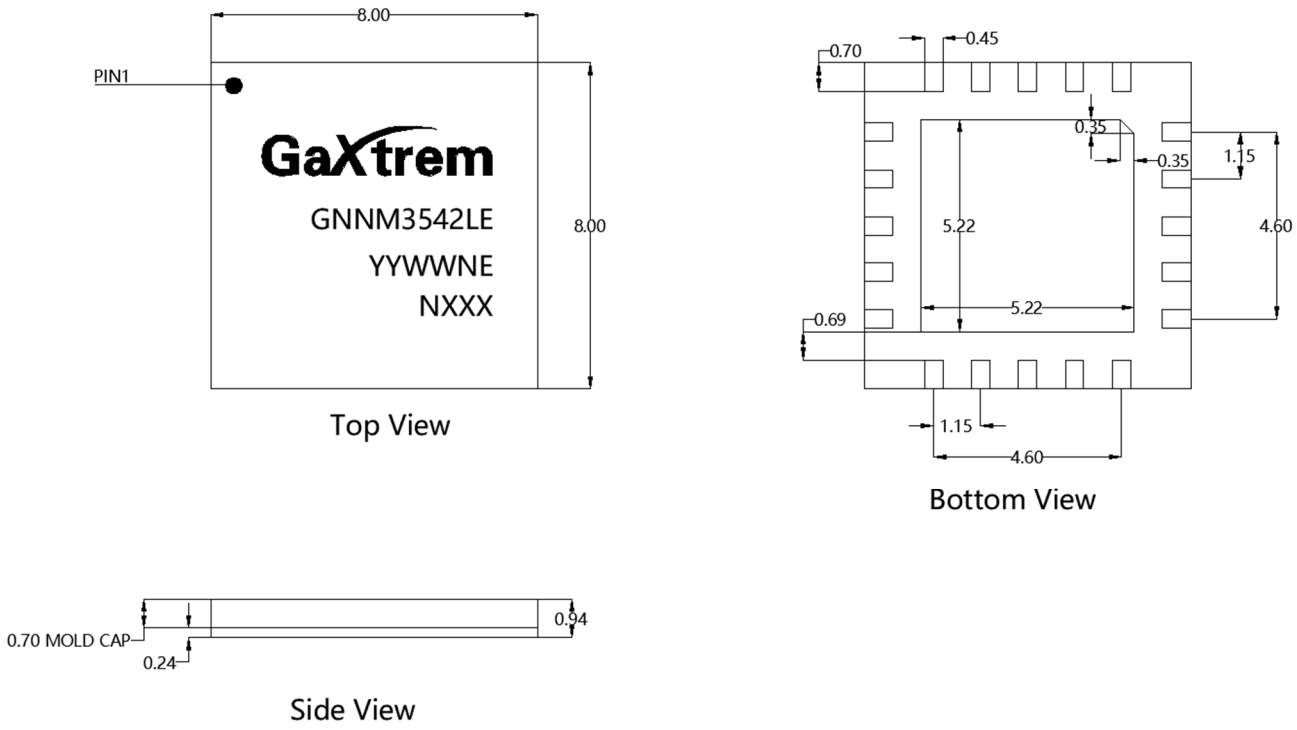

Figure 8. GNNM3542LE Package Dimension

Notes:

1. All dimensions are in millimeters.
2. Exposed metallization is NiPdAu plated.
3. All Edges are 0mm.

MOUNTING FOOTPRINT PATTERN

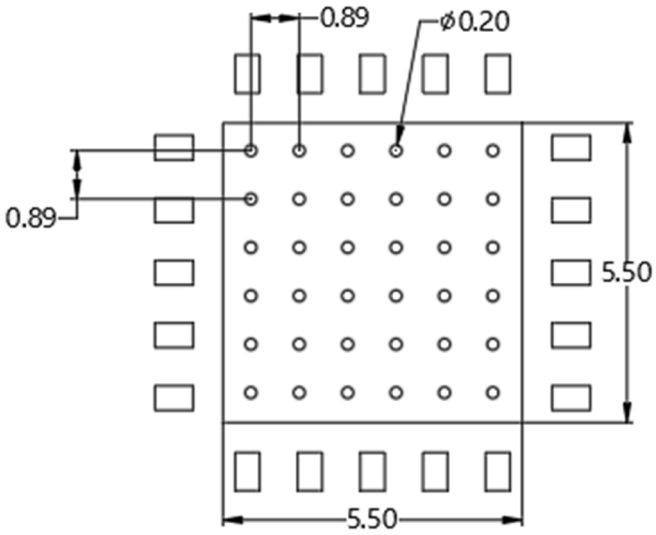

Figure 9. GNNM3542LE PCB Layout Footprint

Notes:

1. All dimensions are in millimeters. Angles are in degrees.

2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. All vias are plated thru hole (PTH) to ground.

RECOMMENDED SOLDER TEMPERATURE PROFILE

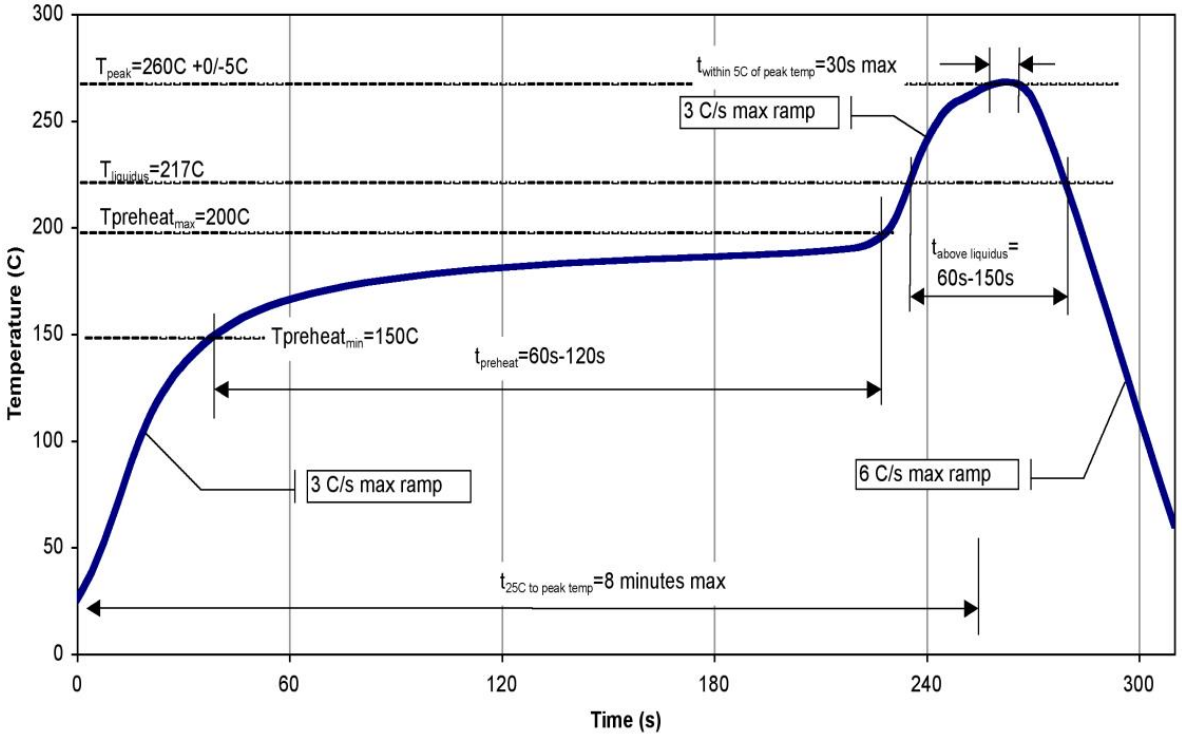

Figure 10. Recommended Solder Temperature Profile

HANDLING PRECAUTIONS

Table 9. ESD Sensitivity

Parameter	Rating	Standard
Human Body Model (HBM)	± 225V	JEDEC Standard JS-001-2017
Charged Device Model (CDM)	± 1000V	JEDEC Standard JS-002-2018

SOLDERABILITY

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiAu

RoHS COMPLIANCE

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

REVISION HISTORY

Table 10. Document Revision History

Date	Revision	Datasheet Status
2023/06/08	Rev 1.0	Preliminary Datasheet
2023/6/28	Rev 1.1	Update measurement results; update application schematic; update ESD sensitivity ; add VSWR mismatch；add gain vs power across temperature.